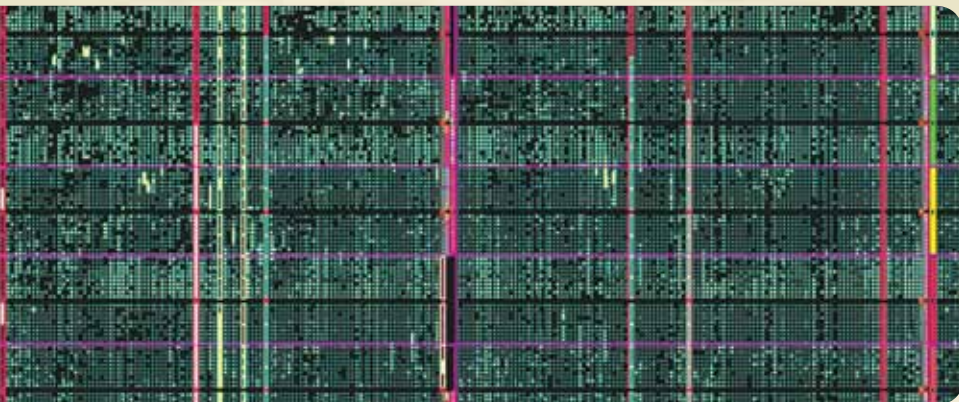


University of South Carolina

INDUSTRY: Emerging Computer Architectures



Heterogeneous and Reconfigurable Computing Research Group focuses on analysis and implementation of computationally intensive applications, employing coprocessors such as FPGAs and GPUs to accelerate applications.



OBJECTIVE

Use emerging computer architectures to accelerate important scientific applications, especially those that are historically difficult to accelerate and those that have never before been accelerated.

APPROACH

Implement new design methodologies for high-performance computing using emerging computer architectures, such as field programmable gate array (FPGA) technologies.

RESULTS

- Developed sparse matrix personality for the Convey HC-1™, achieving 3.4x higher throughput relative to attached GPU.
- Applications involving sparse matrix computations can now achieve a significant acceleration.

A Man on a Mission

USING THE WORLD'S FIRST HYBRID-CORE COMPUTER TO ACCELERATE APPLICATIONS NEVER BEFORE ACCELERATED

Dr. Jason Bakos, associate professor at the University of South Carolina Department of Computer Science and Engineering, is a man on a mission. His goal is to accelerate high performance computing (HPC) applications that have never before been accelerated.

At the University of South Carolina (USC), Bakos leads a team of graduate students in computer science and engineering. Founded in 2000, the Heterogeneous and Reconfigurable Computing Group (HeRC) focuses on uncovering new design methodologies for HPC ranging from developing new automatic CPU/coprocessor partitioning tools to improving system architectures with reconfigurable technologies. The team was one of the first in the world to accelerate computational biology applications with field programmable gate arrays (FPGAs).

"We are attempting to make heterogeneous platforms and associated coprocessor development as ubiquitous as traditional HPC platforms, such as clusters and SMPs and their programming models," explains Bakos.

The World's First Hybrid-Core Computer.

LEARN MORE ABOUT THE WORLD'S FIRST HYBRID-CORE COMPUTER.
VISIT CONVEYCOMPUTER.COM OR CALL 1-866.338.1768

ASBESTOS STUDY

“Heterogeneous platforms offer the potential to achieve a 100x or more performance improvement over traditional systems. Designing custom FPGA-based accelerators is one of the purest forms of applied computer architecture.”

FINDING THE IDEAL RESEARCH PLATFORM

In his quest to accelerate HPC applications, Bakos discovered Convey Computer, a Texas-based company that invented the world’s first hybrid-core computer. The Convey HC-1 combines the low cost and simple programming model of a commodity system with the performance of customized hardware architecture.



At the Supercomputing 2009 tradeshow, Bakos first learned about the Convey HC-1. “I was really impressed. The system had many of the features I was looking for—plenty of memory bandwidth, four state-of-the-art FPGAs, and a coherent memory system. It also had a general purpose and easy-to-use programming model, allowing the host and the coprocessors to communicate and synchronize with one other. Another really nice feature was that the user-programmable FPGAs had direct connections between each other, allowing fast communication between them.”

Bakos’s team works with a wide range of applications that generally require a significant amount of memory, memory bandwidth, and fast interconnects. “We needed all of that, plus we wanted a system that was easy to program, easy to use, and easy to synchronize the host to the coprocessor;” continued Bakos. “The HC-1 was the first platform I had ever seen that could do everything we needed it to do.”

THE WORLD’S FIRST HYBRID-CORE COMPUTER

Convey’s revolutionary hybrid-core computing architecture tightly integrates advanced computer architecture and compiler technology with commercial, off-the-shelf hardware—namely

Intel® Xeon® processors and Xilinx® FPGAs. The company’s solutions, the HC-1 and the HC-1^{EXTM}, help customers dramatically increase performance over industry standard servers. Additionally, Convey systems are easy for programmers to use because they provide full support of an ANSI-standard C, C++ , and FORTRAN development environment.

The University of South Carolina installed the Convey HC-1 in April of 2010. Since that time, the team has been using the system as a platform for characterizing custom-designed computational kernels. “Convey’s FPGA-based coprocessors are extremely flexible and amenable to optimizing algorithms used in computational biology;” said Bakos. “Convey offers a complete system and full support, which allows us to focus on using the machine for our research as opposed to wasting time on getting the machine to work.”

THE HIGH-PERFORMANCE CHALLENGE OF SPARSE MATRIX APPLICATIONS

According to Bakos, his team is using the Convey HC-1 to explore ways to utilize FPGAs as coprocessors for HPC and scientific computing. “We pick out specific applications that we think are important or particularly challenging to adapt for FPGA execution, and then we do a custom implementation,” Bakos explained. “In other words, we hand code and accelerate that particular application.”

Their goal is to demonstrate what kind of performance they can get out of FPGA-based computers on these types of applications as compared to just using software alone (such as shared memory multiprocessors and clusters with message passing type programming models). The team also hopes to expose some challenges, as there are currently no industry standard approaches for taking an arbitrary application and accelerating it with a customized coprocessor.

One of the most exciting things the team accomplished in the past year using the HC-1 was to develop a sparse matrix personality. Convey’s personalities are instruction sets designed specifically to achieve orders of magnitude acceleration in a variety of applications. Convey currently licenses several personalities, but none for sparse matrix computations.

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—Dr. Jason Bakos, associate professor,
University of South Carolina
Department of Computer Science and Engineering

In science and engineering, sparse matrix computations are algorithms that work on huge matrices whose elements are primarily zero. In order to store sparse matrices on a computer, the data is usually compressed, only keeping nonzero elements. To manipulate a sparse matrix computation accurately, algorithm designers must first deal with the compressed format, which is computationally demanding.

Bakos and his team used the Convey Personality Development Kit (PDK) to create a new architecture for sparse matrix algorithms. The result was an acceleration of 1.4x up to 3.4x compared to a state-of-the-art GPU-based coprocessor, depending on the matrix they tested. With this new personality, anyone doing simulations using sparse matrix computations—from weather to electrical systems—can now achieve a significant acceleration of their application.

THE PAPER IS PUBLISHED AND THE EXCITEMENT BUILDS

Bakos and another team member, Krishna K. Nagar, detailed their work in a paper presented at the 19th Annual IEEE International Symposium on Field-Programmable Custom Computing Machines on May 2, 2011. The paper entitled, “A Sparse Matrix Personality for the Convey HC-1,” generated a great deal of excitement among the organizers and participants.

“I think everyone was extremely excited to see our results, because we demonstrated that a FPGA-based

coprocessor can achieve higher acceleration than a GPU-based coprocessor,” continued Bakos. “We took a professional class GPU platform, ran it against our personality on the HC-1, and we achieved 3.4x speed up.”

According to Bakos, this result is especially interesting because GPU-based solutions are known to achieve their best results on traditional scientific applications that rely on numerical linear algebra methods, including sparse matrix computations. In contrast, FPGA solutions are known to perform better on non-numerical applications, such as combinatorial, graph-based, and other control-dependent computations. “To see such acceleration on a traditional application gives us confidence that with continued research, we will achieve even greater acceleration using the HC-1 with non-numerical scientific applications.”

ADDITIONAL COMPUTATIONAL BIOLOGY RESEARCH

Beyond working with new computer architectures, Bakos and his team are using the Convey HC-1 to speed up applications ranging from computational phylogenetics to data mining and logic minimization. They develop non-traditional applications such as computationally intensive phylogenetics inference methods. Computational phylogenetics, which studies the evolutionary development of a species or group of organisms, involves the search for the most accurate “evolutionary tree” from a space of possible trees. The search space grows exponentially with the number of inputs, going from 2 million possible trees for 10 species to 25 trillion quadrillion (2.5×10^{28}) possible trees for just 25 species.

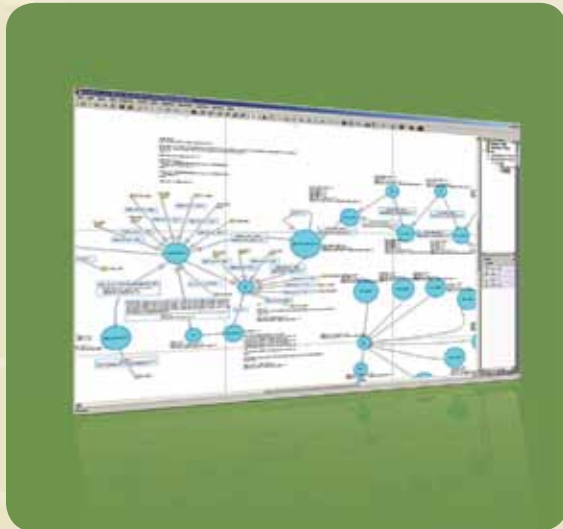
Aside from the size of the search space, assessing the accuracy of each candidate tree itself involves complex methods in order to match a specific tree to its evolutionary model—a computationally expensive operation. By studying the past and building accurate phylogenetic trees, scientists are able to more quickly identify treatments to combat everything from an emerging virus to pesky weeds growing in a front yard.

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"A GOOD FPGA DESIGN CAN PROVIDE ONE TO THREE ORDERS OF MAGNITUDE SPEED-UP OVER A TRADITIONAL CPU." —DR. BAKOS



ABOUT CONVEY COMPUTER CORPORATION

Based in Richardson, Texas, Convey Computer breaks power, performance, and programmability barriers with the world's first hybrid-core computer—a system that marries the low cost and simple programming model of a commodity system with the performance of a customized hardware architecture. Convey brings decades of experience and intellectual assets to performance problem solving. Its executive and design teams all come from successful backgrounds of building computer companies, most notably Convex Computer Corporation and Hewlett-Packard. More information can be found at: www.conveycomputer.com.

ABOUT THE HETEROGENEOUS AND RECONFIGURABLE COMPUTING GROUP

The Heterogeneous and Reconfigurable Computing Group at the University of South Carolina (herc.cse.sc.edu) was founded in 2000 by Dr. Duncan Buell, a pioneer in the field of high-performance reconfigurable

computing. Dr. Jason Bakos succeeded Dr. Buell as the group's leader in 2005 and, under his leadership, the group was one of the first in the world to accelerate computational biology applications with FPGAs and was the first to accelerate parsimony-based phylogeny reconstruction. The group actively publishes in several IEEE Computer Society transactions and participates in the world's largest FPGA conferences.



Dr. Jason Bakos

The group is funded by the National Science Foundation under grants CCF-0844951 and CCF-0915608, and is part of the Department of Computer Science and Engineering in the College of Engineering and Computing at the University of South Carolina.