

For more information at ISC'09, please contact:

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Convey Computer™ Corporation Ships First Hybrid-Core Computers

RICHARDSON, TX (June 23, 2009) – Convey Computer Corporation announced at the International Supercomputing Conference (ISC'09) that the company is shipping beta units of its hybrid-core computing system, the Convey HC-1™. Beta test applications include bioinformatics, data mining, government/defense, and oil and gas.

Created by the executive team that built Convex Computer, Convey is developing a new solution for CPU-intensive applications called hybrid-core computing. Hybrid-core computing marries the low cost and simple programming model of a commodity system with the performance of customized hardware architecture.

The Convey HC-1 integrates advanced, patent-pending computer architecture and compiler technology with commercial, off-the-shelf hardware – namely an Intel® Xeon® processor and Xilinx® Field Programmable Gate Arrays. The HC-1 features a Convey-engineered coprocessor with its own high-bandwidth, virtual memory addressed, cache-coherent memory subsystem in a scalable 2U chassis. Moreover, an ANSI standard development environment gives programmers 100 percent productivity and portability – an attribute unique to Convey.

The HC-1 transforms HPC in three main ways. It: 1) breaks through the current power/performance wall to significantly increase performance for certain compute and memory bandwidth intensive applications within bioinformatics, financial analytics, seismic, and certain other application areas; 2) is easy for programmers to use because

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it provides full support of an ANSI-standard C, C++ and Fortran development environment; and 3) significantly reduces support, power and facility costs for companies.

The HC-1 will be on display at ISC'09, Booth 702. Additionally, Steve Wallach, co-founder of Convey Computer and 2008 winner of the Seymour Cray Computer Science and Engineering Award, will present "*A New HPC Architecture: Hybrid-Core Computer*" on Friday, June 26, at 9 a.m.

Bruce Toal, president and CEO of Convey Computer Corporation, said that since the company's introduction in November 2008 potential customers "are very excited about both the innovative hybrid-core architecture as well as the potential energy savings – up to 92 percent lower power and cooling costs – that the systems deliver." Early customers of the technology agree. The University of California, San Diego (UCSD) has placed the first order under its Project GreenLight power and energy efficiency initiative, and estimates substantial performance gains and cost savings.

"The HC-1 is a remarkably ingenious and innovative HPC architecture, which combines the best of both worlds of general purpose multi-core and special-purpose Field Programmable Gate Arrays," said Dr. Larry Smarr, director of the California Institute for Telecommunications and Information Technology (Calit2) and a professor of Computer Science and Engineering in UCSD's Jacobs School of Engineering. "Once again, Steve Wallach has introduced a new class into HPC architectures."

About the Convey HC-1

The technology breakthroughs and key competitive strengths of the HC-1 include:

- **Hybrid-core architecture** – Instructions executed by the coprocessor appear as extensions to the x86 instruction set, sharing the same physical and virtual address spaces, and applications can contain both x86 and coprocessor instructions in a single-instruction stream. Supporting this, the Convey compilers generate one executable image that contains both x86 and coprocessor instructions.

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- **Personalities** – Customized instruction sets increase productivity for specific HPC applications. 32-bit complex arithmetic instructions, for example, would boost performance for seismic processing. Systems can contain multiple personalities. A Personality Development Kit (PDK) allows for creation of new application-oriented architectures. Convey is designing personalities for key applications in bioinformatics, computer-aided design, financial services, and oil and gas.
- **Adaptable architecture** – The server adapts to the application to maximize computing efficiency and flexibility. Personalities are demand-loaded upon process startup, making Convey servers flexible in mixed-use environments.
- **Memory** – Memory bandwidth of 80 Gigabytes/sec delivers huge sustainable performance. A shared virtual and physical memory between the coprocessor and the x86 provide the tight integration that allows the system to be programmed as a single architecture. This means that the programmer does not need to manage the physical memory on the coprocessor nor explicitly move data back and forth between the x86 main memory and the coprocessor main memory.
- **Easy programming** – Application development, including coding, debugging and deployment, relies on ANSI standard C, C++ and FORTRAN development tools.
- **Easy cluster integration** – The development and runtime environments are based on the Linux® operating system for easy integration into existing x86 clusters.

About Convey Computer Corporation

Based in Richardson, Texas, Convey Computer breaks power, performance and programmability barriers with the world's first hybrid-core computer—a system that marries the low cost and simple programming model of a commodity system with the performance of a customized hardware architecture. Convey brings decades of experience and intellectual assets to performance problem-solving. Its executive and design teams all come from successful backgrounds of building computer companies, most notably Convex Computer Corporation and Hewlett-Packard. Convey Computer investors include CenterPoint Ventures, Intel Capital, InterWest Partners, Rho Ventures, and Xilinx. More information can be found at: www.conveycomputer.com.

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